

Comp 411 Computer Organization
Spring 2012

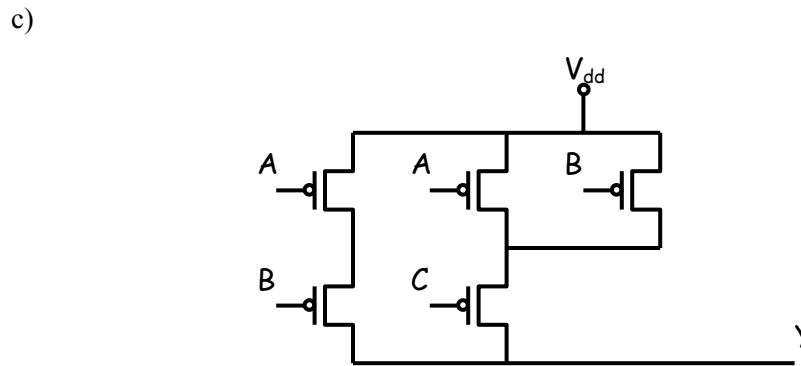
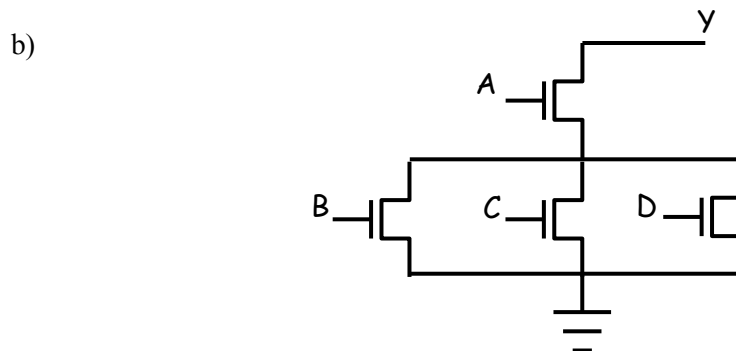
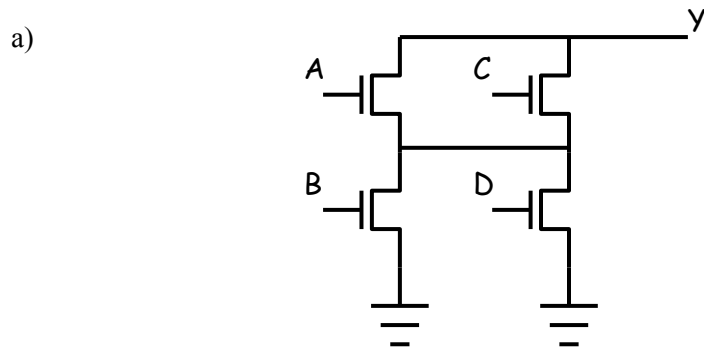
Problem Set #3

Issued Wednesday, 2/15/12; Due Wednesday, 2/29/12

Homework Information: Some of the problems are probably too time consuming to be done the night before the due date, so plan accordingly. Late homework will not be accepted. Feel free to get help from others, but the work you hand in should be your own.

Problem 1. “Fishing for Complements”

Show the complementary set of p-channel or n-channel transistors that complete the following CMOS circuits:

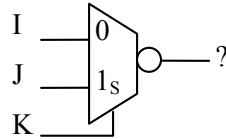


Problem 2. “Table Manners”

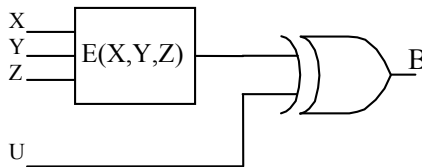
Inputs			Outputs				
X	Y	Z	A	B	C	D	E
0	0	0	1	0	1	1	0
0	0	1	0	0	1	1	0
0	1	0	1	0	1	1	0
0	1	1	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	1	0	0
1	1	0	0	1	0	0	0
1	1	1	0	0	0	1	1

The following questions refer to the truth table above, which specifies five Boolean functions, A, B, C, D, and E.

- a) Which functions can be realized by the following logic diagram and *no additional* logic? For each, show how to connect one of X, Y, Z, 0, or 1 to I, J, and K.



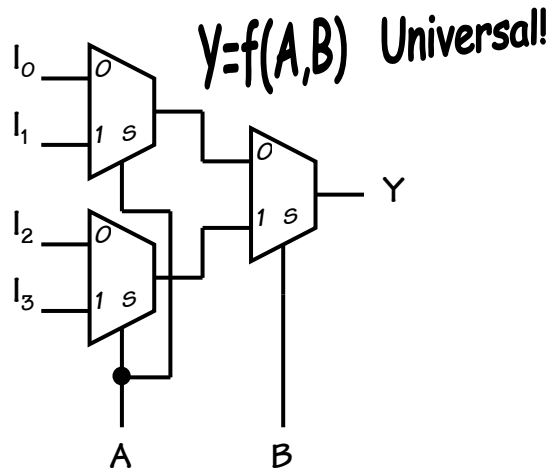
- b) Which functions from the table can be implemented using only a single 2-input multiplexor without invertors on any input or output?
- c) Which functions can be implemented as a single-level CMOS gate?
- d) An implementation of function E can be used to compute function B with the following circuit, if the unknown input, U, is properly connected.



What signal should be connected to U?

Problem 3. Mux Madness

During a particularly boring Comp 411 lecture about the universality of NAND and NOR gates, Lee Hart suddenly realizes that multiplexers are also universal. At the close of lecture he awakes and jots the following diagram on the back of his lecture notes:



Help explain Lee's insight.

- Give binary values for I_0 , I_1 , I_2 , and I_3 which implement the following functions on the two inputs A and B: AND(A,B), OR(A,B), XOR(A,B), NAND(A,B), and NOR(A,B).
- Can every 2-input Boolean function be implemented using Ben's structure? Explain why or why not.

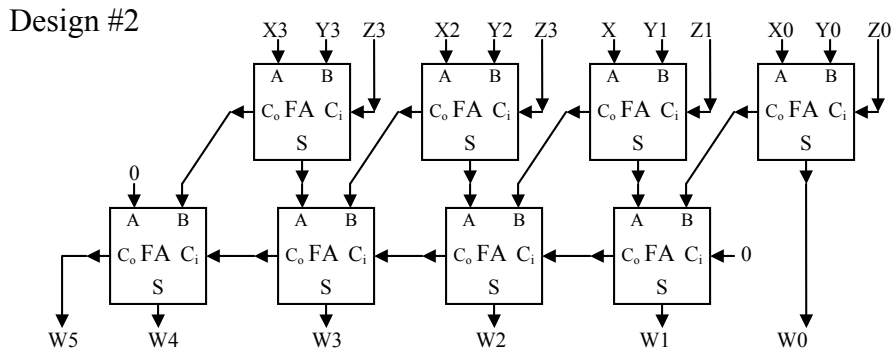
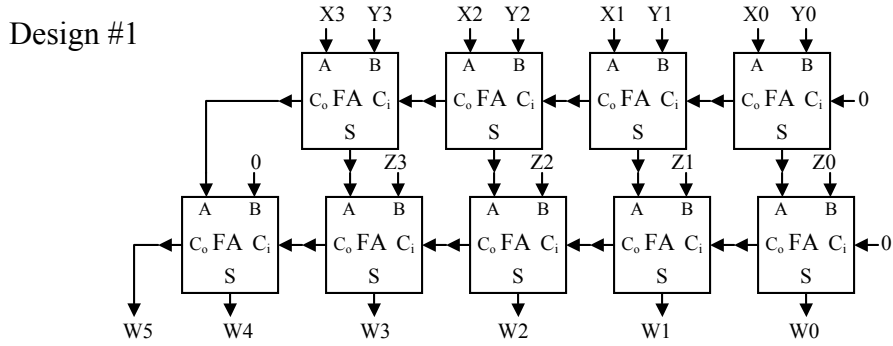
The next day, in an effort to impress his TA, Lee attends office hours and explains his discovery. He decides to make his point by constructing several standard gates using his structure. Not to be out done, the TA claims that he could build each 2-input gate using only 2 multiplexers.

- Show how to implement an inverter, as well as every 2-input gate using no more than 2-multiplexers to construct each one.
- Explain how every 4-input Boolean function can be implemented with an 8-input mux and a single inverter.

The TA explains to Lee that no more than 40% of all 4-input Boolean functions can be implemented with only an 8-input mux (i.e. no inverter). He jots down an upper bound on the number of such functions: $3^8/2^{14}$. Can you explain the TA's reasoning?

Problem #4. “An Adder’s Bite”

Consider the follow two circuits for adding 3, 4-bit numbers (i.e. $W = X + Y + Z$):



- Ignoring the speed of the calculation, do both 3-input adder designs eventually compute the same result? If not, how do they differ?
- Assume a unit delay for each full-adder (i.e. the output will become valid one time unit after all inputs are valid). Which design computes all bits of the sum fastest? Which design computes the first (least-significant) bit fastest?
- Obviously, design #1 uses one more adder than design #2. Explain how design #1 can be modified slightly to use one fewer full-adder. After this change, which design computes all bits of its sum fastest?
- Both designs could be improved by incorporating carry-lookahead logic in place of their carry-propagation chains. Which design would requires less logic to implement carry lookahead? Explain.
- Modify both designs to support the following operations:

$$W = X + Y + Z \quad \text{or} \quad W = X + Y - Z,$$

based on the value of a control signal (CTRL). Draw a schematic of your design.